IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Hidemi TSUNODA, residing at 1-12-7, Misaka, Shirakawa-shi, Fukushima-ken, 961-0836 Japan, declares:

(1) that he knows well both the Japanese and English languages;

(2) that he translated the Japanese document entitled "Measuring Method, Measurement-Signal Output Circuit, and Measuring Apparatus" from Japanese to English;

(3) that the attached English translation is a true and correct translation of the above-identified Japanese document to the best of his knowledge and belief; and

(4) that all statements made of his own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: March 31, 2004

H. Tsunoda

Hidemi TSUNODA